

This paper examines the problem of code generation for expression trees on non-homogeneous register set architectures. It proposes and proves the optimality of an  $O(n)$  algorithm for the tasks of instruction selection, register allocation and scheduling on a class of architectures defined as the  $[1, \infty]$  model. Optimality is guaranteed by sufficient conditions derived from the register transfer graph (RTG), a structural representation of the architecture which depends exclusively on the processor instruction set architecture (ISA). Experimental results using the TMS320C25 as the target processor show the efficacy of the approach.