RISC processors can be used to face the ever increasing demand for
performance required by embedded systems. Nevertheless, this
solution comes with the cost of poor code density. Alternative
encodings for instruction sets, such as MIPS16 and Thumb, represent
an effective approach to deal with this drawback. This article
proposes to apply a new encoding to the SPARCv8 architecture.
Through extensive analysis of a program mix from the Mibench and
Mediabench benchmark suites, we suggest a new 16-bit instruction
set, easily translated to its 32-bit counterpart during execution
time. Using the aforementioned program mix to infer how code could
be represented in the proposed 16-bit ISA, compression ratios as low
as 56% can be obtained. We also evaluated the cache behavior and
showed reductions of 42% on cache misses that can increase
performance up to 28% (for patricia program with 2KB cache).