

Transactional memory (TM) is an emerging synchronization mechanism that aims to solve most of the difficulties inherent in lock-based approaches. TM implementations may either rely on special hardware (HTM) or employ a software-only (STM) technique. While STM can be implemented and evaluated in current machines, HTM requires hardware modification and a prototyping infrastructure. We present in this paper a flexible platform framework for rapid prototyping and evaluation of HTM systems. Platform components such as cache, memory and interconnection medium are implemented using SystemC and Transaction-Level Modeling (TLM). Processors are described in an Architecture Description Language (ADL) which makes it practical to change the Instruction Set Architecture (ISA), since simulators and binary utilities are automatically generated by the ADL toolset. The resulting flexibility allows designers to explore the design space in a simple and uniform manner. We illustrate the platform through a case study based on the original HTM proposed by Herlihy and Moss. Simulation results are shown for microbenchmarks supporting up to 256 processors.