

The new design challenges imposed by the increasing difficulties of today's electronic systems obligated designers to develop new methodologies. System-level design and platform-based design are playing an important role in the electronics industry, and design reuse is a key concept. SystemC is a design language which is being largely adopted to raise the abstraction level of hardware design and verification, becoming an important system design language nowadays. Considering the large amount of VHDL RTL modules already available and that systems design are hardly ever started from scratch, co-simulating VHDL and SystemC hardware modules becomes very desirable. This paper presents a new methodology, based on an open-source toolset (libraries and programs), to co-simulate SystemC and VHDL components. We use a platform case study to measure simulation performance and compare our infrastructure to Modelsim.