A retargetable VLIW compiler framework for DSPs with instruction-level parallelism,

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- DSP chips
- Fujitsu Hiperion fixed-point DSP
- SoC design
- assembly code generation
- digital signal processor
- embedded processors
- enhanced IMPACT framework
- execution time improvement
- highly retargetable optimizing compilers
- instruction-level parallelism
- irregular architectures
- retargetable VLIW compiler framework
- system-on-a-chip design
- very long instruction word processor
- digital signal processing chips
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- instruction sets
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- parallel architectures

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